ECE6332 Project Design Review II

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1 Simulation Results

In this project, two circuits, a single inverter and a ripple carry adder, are simulated and studied over a set of PTM technology libraries from 45nm down to 16nm, both variants of high-performance (HKMGS) and low-power (LP) are covered. The nominal voltage and threshold voltage for each technology libraries are listed in Table 1.

		$45nm$	$32nm$	$22nm$	$16nm$
High Perf.	V_{nom} (V)	1.0	0.9	0.8	0.7
	V_{th} (mV)	424.25	466	508.16	504.9
Low Power	V_{nom} (V)	1.1	1.0	0.95	0.9
	V_{th} (mV)	622.61	647	707.3	710.32

Table 1: Nominal supply voltage and threshold voltage for each PTM technology library

Propagation delay, switching power and static leakage power are the metrics of interest in this project. The propagation delay is measured from the time input has changed by 50% (t_{in}) to the time output has changed by 50% (t_{out}), which is shown as:

$$T_p = t_{out} - t_{in} \tag{1}$$

$$P_{dyn} = vdd \cdot \int_{t_{in}}^{t_{out}} I_d \, dt \Big/ T_p \tag{2}$$

$$P_{lkg} = vdd \cdot (\int I_d \, dt - \int_{t_{in}}^{t_{out}} I_d \, dt) \Big/ (T_{sim} - T_p) \tag{3}$$

1.1 Inverter

The schematic of the circuit is shown in Figure 1

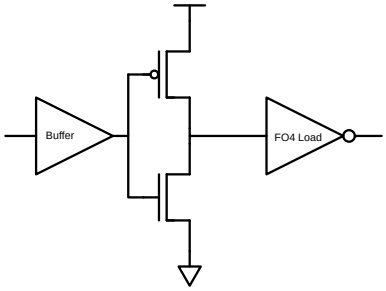
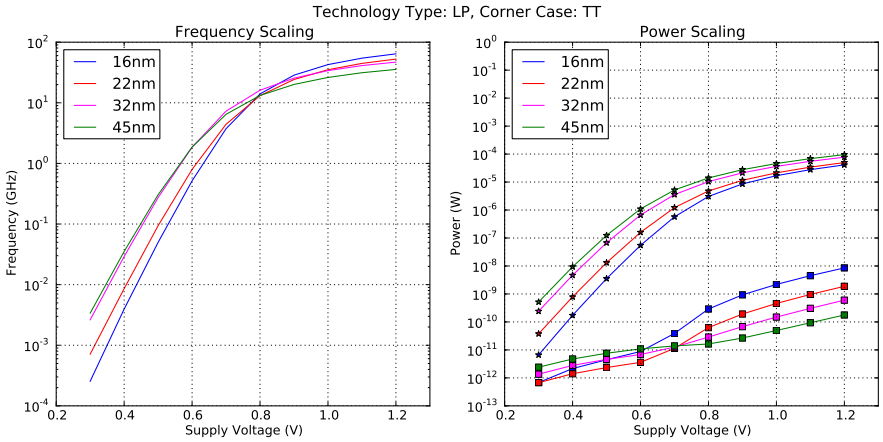
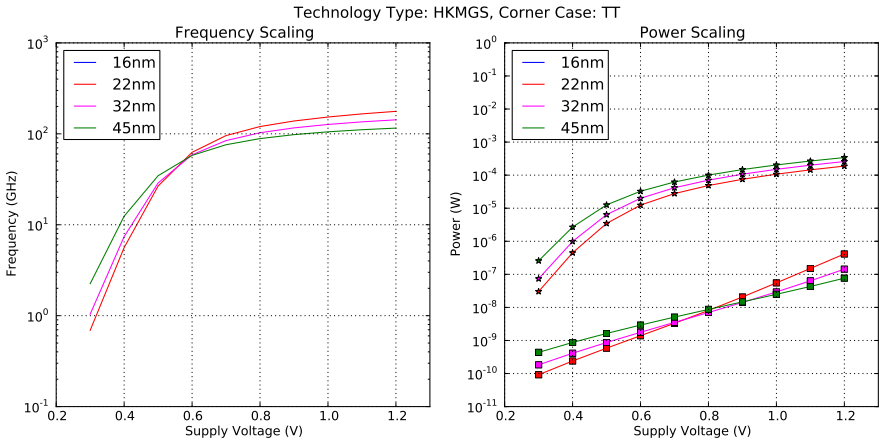


Figure 1: Schematic of an inverter, along with its driving buffer and output load

I first simulate the circuit with supply voltage sweeping from nominal to threshold for each technology nodes. Results are shown in Figure 2



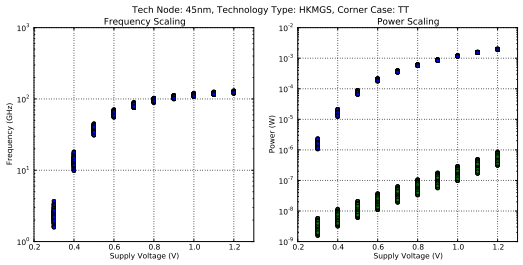
(a) Low-power process



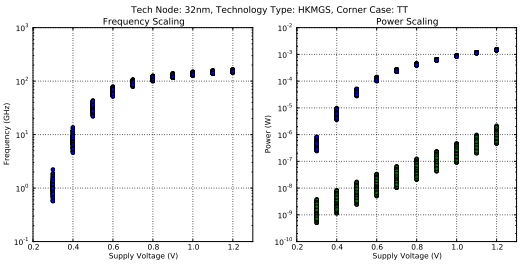
(b) Hihg-performance process

Figure 2: Supply sweeping on a single inverter

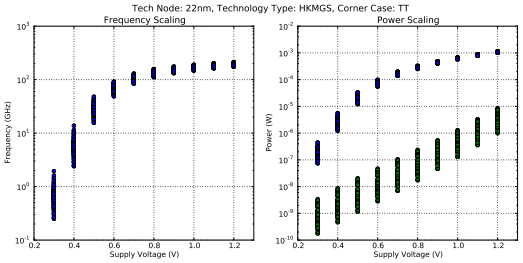
I then conduct the Monte Carlo simulation on the inverter circuit, results are shown in Figure 3 and Figure 4 for high-performance process and low-power process, respectively.



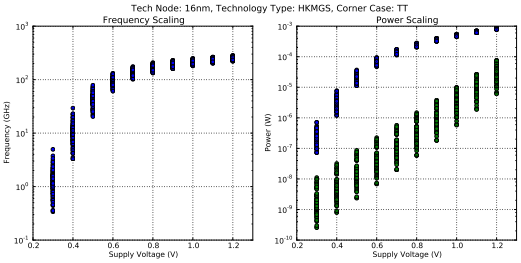
(a) 45nm



(b) 32nm

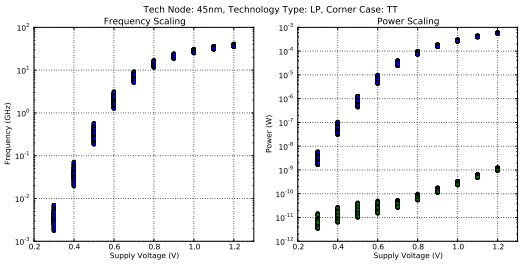


(c) 22nm

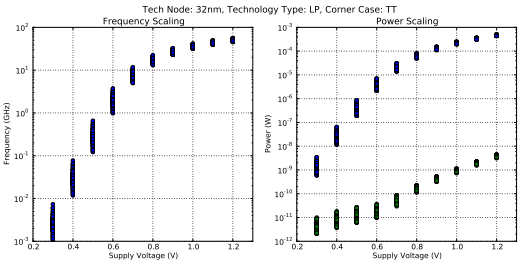


(d) 16nm

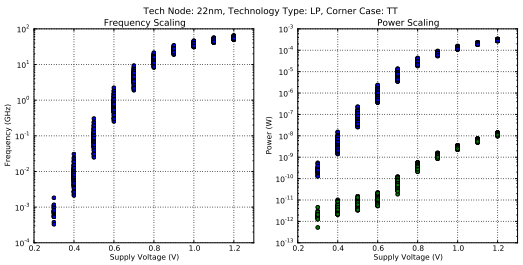
Figure 3: Monte Carlo simulation with high-performance process



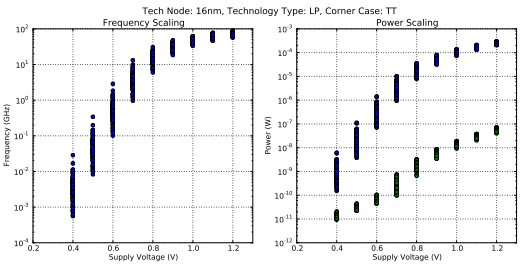
(a) 45nm



(b) 32nm



(c) 22nm



(d) 16nm

Figure 4: Monte Carlo simulation with low-power process

1.2 Adder

A simple ripple carry adder is chosen for this project, the schematic of the circuit is shown in Figure 5

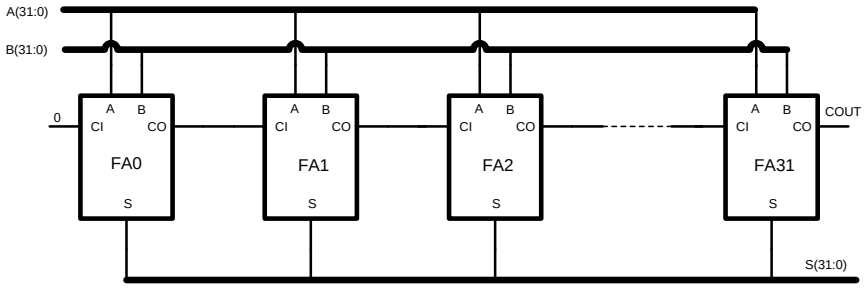
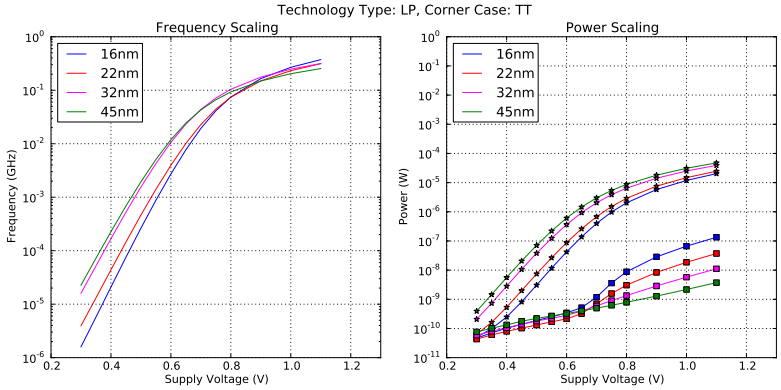
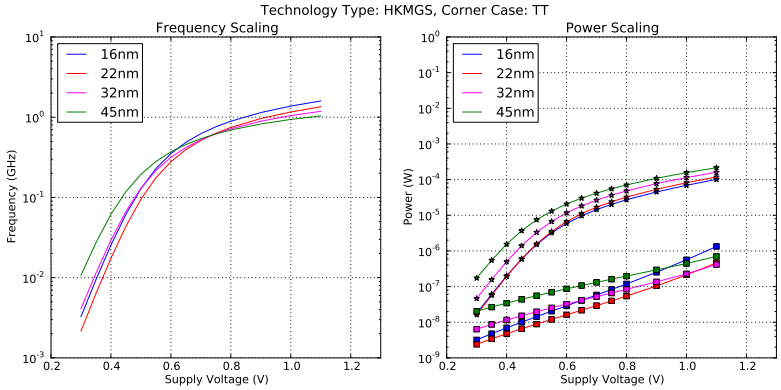


Figure 5: Schematic of a 32-bits ripple carry adder

I simulate the adder circuit sweeping the supply, the results are shown in Figure 6



(a) Low-power process



(b) High-performance process

Figure 6: Supply sweeping on a ripple carry adder

2 Report

The project progress so far is on the track. I have finished normal simulations and Monte Carlo simulations on inverter circuit. Normal simulations on adder circuit have been finished as well. Monte Carlo simulations on adder are still running.

One of the most challenging tasks I have faced is the Monte Carlo simulation time. Referred to wiki tutorial, I firstly modified the normal simulation script to Monte Carlo simulation using 'monteExpr' function call to evaluate the delay and power of the circuit. However, I failed in this way because 'monteExpr' function call did not support variables to be part of the evaluation expressions. Due to this limitation, I had to setup a Monte Carlo simulation for one single iteration each time, then computed delay and power. After all these expressions were all evaluated and exported into a file, I started the next iteration of Monte Carlo simulation a new setup. Although the simulations went through and generated all data as expected, it suffers from severe speed issue. I have compared the running time of the iteration-by-iteration Monte Carlo simulation with typical one-launch simulation, my current approach was 3 times slower than the typical way with 10 iterations on a single inverter circuit.

The remaining tasks are:

1. Finish Monte Carlo simulation on adder.
2. Figure out how to mimic different circuit activity factors by composing circuits with adders.
3. Simulate those circuits.